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Investigation of the effect of temperature during off-state degradation of AlGaN/GaN High Electron Mobility Transistors

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ABSTRACT

AlGaN/GaN High Electron Mobility Transistors were found to exhibit a negative temperature dependence of the critical voltage (V_{CRI}) for irreversible device degradation to occur during bias-stressing. At elevated temperatures, devices exhibited similar gate leakage currents before and after biasing to V_{CRI}, independent of both stress temperature and critical voltage. Though no crack formation was observed after stress, cross-sectional TEM indicates a breakdown in the oxide interfacial layer due to high reverse gate bias.

1. Introduction

AlGaN/GaN High Electron Mobility Transistors (HEMTs) have attracted interest due to their high performance capabilities. For this technology to become a key component for high frequency and high power applications, there is a need to understand the degradation mechanisms that affect the long-term reliability. Employment of GaN HEMTs for applications such as high power radar systems will require devices to be driven into saturation while being subjected to large-signal RF, resulting in devices experiencing high electric fields and high current densities. For example, Campbell and Dumpka have reported upwards of 40 W of off-state power for single pole double throw GaN on SiC switches with a gate bias of −37 V for source-to-drain spacing of 4 μm, similar to the devices studied here [1]. A dc gate bias step stress permits one to isolate the effect of high electric field on the Schottky contact, which has been investigated in detail by several groups [2–15]. However, there has been no study on the interacting effects of temperature and high reverse dc gate bias on the Schottky contact to the author's knowledge.

During a high reverse gate bias step stress, gate leakage current in AlGaN/GaN HEMTs is seen to steadily increase, until critical voltage (V_{CRI}) is reached [2,3,6,9,11,12]. At this point, the gate leakage current sharply increases about 1–2 orders of magnitude. This sharp rise in current has been attributed to the inverse piezoelectric effect [6,11,12]. As the electric field increases, the tensile stress in the AlGaN layer increases. Added on top of the intrinsic tensile strain, it is believed that at the critical voltage, crystallographic defects form from the excessive mechanical strain, creating both electron traps and increasing electron tunneling through the defect states [4,6,7,12,14–18]. Though our devices exhibit electrical characteristics during and after performing the gate step stress that are similar to previously reported results, the formation of cracks at the gate edge have not been observed in our studies [2,3]. In order to further investigate and understand the degradation mechanisms causing the increase in gate leakage current under high reverse gate bias, this paper reports on the temperature dependence of critical voltage.

2. Experimental

AlGaN/GaN HEMTs were fabricated on 6H SiC semi-insulating substrate, beginning with a 2.25 μm Fe-doped GaN buffer layer grown on top of an AlN nucleation layer (Fig. 1A). This was followed by 15 nm of $Al_{0.28}Ga_{0.72}N$, capped with 3 nm of unintentionally doped GaN. On- wafer Hall measurements showed a sheet carrier concentration, sheet resistance, and mobility of 1.06×10^{13} cm^{-2}, 310 Ω/square, and 1900 cm^2/V s, respectively. An inductively coupled plasma mesa etch of ~1000 Å was performed to isolate neighboring devices. Ti/Al/Ni/Au Ohmic metallization was annealed at 850 °C for 30 s for source/drain contacts. The HEMTs employed a Ni/Au double gate design with a gate width of 150 μm, source-to-gate and gate-to-drain distances of 2 μm and were passivated with SiN_x deposited by plasma enhanced chemical vapor deposition (Fig. 1B).

Over twenty identical neighboring HEMTs from a single wafer with a gate length of 0.14 μm were stepped stressed with a HP 4156C semiconductor parameter analyzer from −10 V to −42 V in 1 V increments for 60 s each step in the dark at different

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14. ABSTRACT
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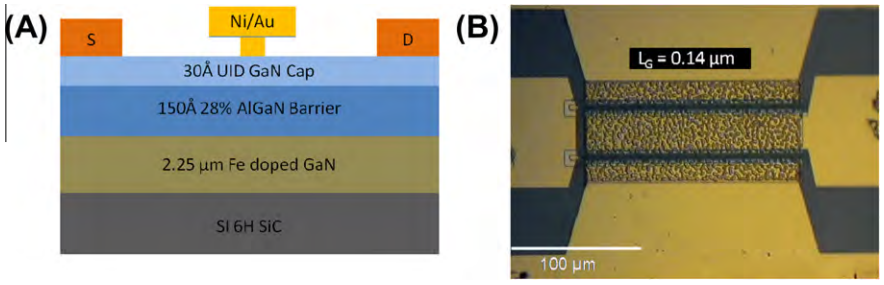

Fig. 1. (A) Optical microscope image of AlGaN/GaN HEMT with gate length (L_G) of 0.14 μm. (B) Cross-section diagram of device structure.

temperatures ranging from 24 °C to 150 °C. The temperature of the devices was regulated by a heated chuck, with at least two devices stressed at each temperature. Pre-stress electrical characteristics were taken at ambient temperature in order to verify that the selected devices exhibited similar performance. The gate current (I_G), gate-to-drain leakage current (I_{GD}), and gate-to-source leakage current (I_{GS}) were monitored during the stressing. Additionally, gate current in the off-state, I_{GOFF}, was measured after each step with a bias of V_{DS} = 0.2 V and V_{GS} = −5 V. Drain and gate current–voltage sweeps were measured pre- and post-stress at room temperature. The device was heated to the desired stress temperature before the step-stress was performed, with gate leakage current, drain and gate *I–Vs*, and extrinsic transconductance being measured at elevated temperatures after each step of the stress test. Both source and drain were held at ground in order to symmetrically stress the gate contact. Furthermore, numerical device simulations (ATLAS/Blaze) were carried out to determine the maximum electric field present in the GaN cap layer at the edge of the gate contact (both source and drain side since the device is symmetrically stressed) when critical voltage is reached.

3. Results and discussion

For all devices, gate leakage current steadily increases as the step-stress is carried out until the critical voltage (V_{CRI}) is reached, upon which permanent degradation of I_G occurs and abruptly increases about an order of magnitude. At room temperature, the HEMTs show a considerable increase (four to five orders of magnitude) in gate leakage current after step-stressing to −42 V (Fig. 2). However, the total gate current increase is less significant after stress at increased temperature (Fig. 3). The increase in I_G after high reverse gate bias has been previously reported and correlated to an increase in drain and source resistance as well as a decrease in saturated drain current, which was also observed in our devices (Fig. 4) [4,6,7,11,12].

The critical voltage of our devices at 24 °C is −30 V. As the temperature of the devices is increased to 150 °C, the critical voltage is observed to linearly decrease (Fig. 5). Error bars shown in Fig. 4 indicate the small variations in critical voltage observed across the region of wafer in which the devices were located, likely due to slight variations in epitaxial layers [19] . Due to the fact that V_{CRI} occurs at lower voltages as the temperature increases, the maximum electric field present at the edge of the gate at V_{CRI} also decreases. ATLAS/Blaze electrical simulations indicate that the peak electric field decreases from 3.3 MV/cm at a critical voltage of

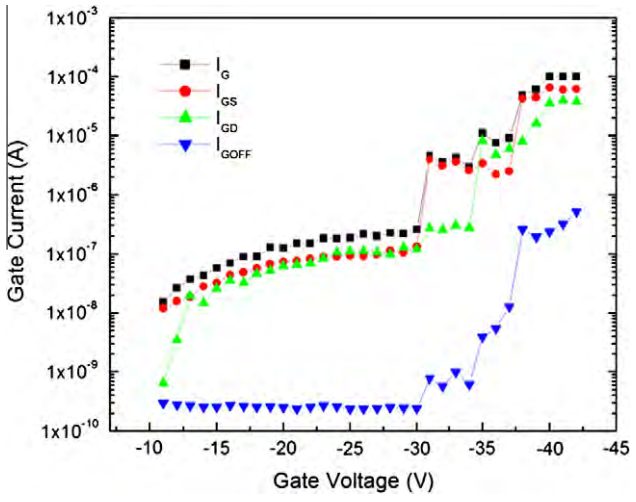

Fig. 2. Gate current of typical device during off-state step stress at room temperature.

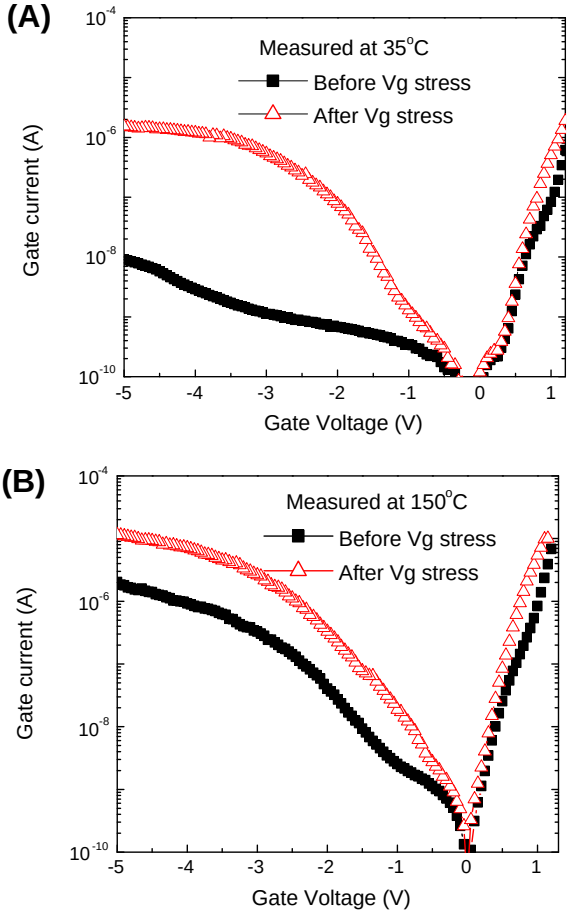

Fig. 3. Gate current–voltage characteristics of 0.14 μm gate length HEMT before and after step-stressing at (A) 35 °C and (B) 150 °C.

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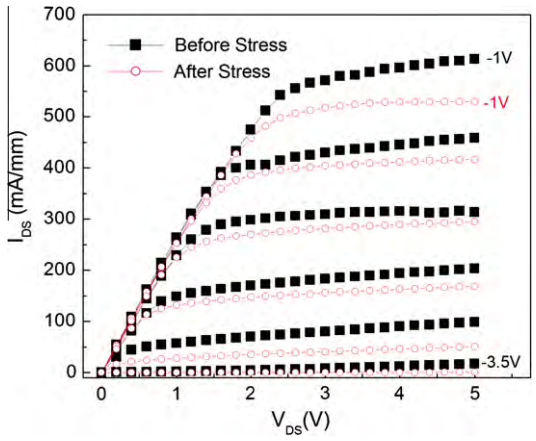

Fig. 4. Drain current–voltage characteristics of a typical device before and after off-state stress test at 24 °C.

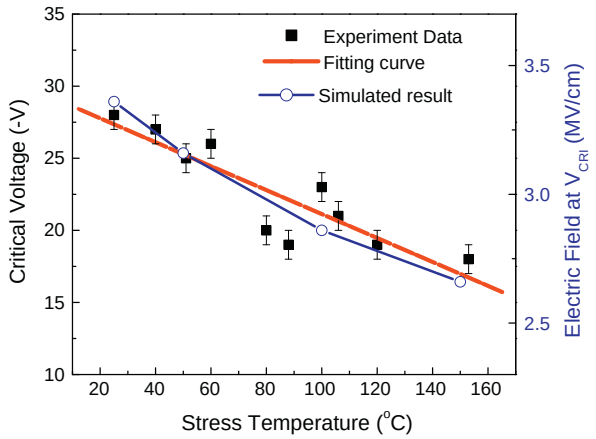

Fig. 5. Stress temperature vs. critical voltage of 0.14 μm gate length HEMT, and stress temperature vs. maximum electric field at the edge of the Schottky contact when critical voltage occurs determined by ATLAS/Blaze 2D simulations.

−28 V with a stress temperature of 28 °C to 2.6 MV/cm at a critical voltage of −18 V at 150 °C (Fig. 6). The gate leakage current measured during the step stress of four different devices stressed at four different temperatures ranging from 24 °C to 150 °C (Fig. 7) further illustrate the negative temperature dependence. Previous reports in the literature attribute the sharp rise in I_G at the critical voltage and resulting permanent I_G degradation to the inverse piezoelectric effect [2,6,7,9,11,12,15,20]. However, this result reveals that the breakdown which results in a sharp increase in gate leakage current does not occur at the same electric field, and therefore does not occur at the same piezoelectric induced stress.

Upon closer examination, one can see that the gate leakage current is independent of critical voltage, (Fig. 8). In addition, a linear fit of gate current indicates that there is no change in I_G as a function of stress temperature (Fig. 9) either at the critical voltage or just above critical voltage (V_{CRI} – 1 V). Error bars in Figs. 8 and 9 were calculated based on the variations of current measured during the step stress and variations across the region of the wafer in which the devices were located. Devices stressed at room temperature have been reported to display a significant dependence on gate voltage/electric field [2,4,6,7,9,11,12,15,18,20]. Ni/Au metallization schemes for Schottky contacts on GaN have been determined to be thermally unstable above 400 °C, with numerous nickel nitrides reported being formed at temperatures as low as 200 °C [21–23]. Additionally, thermal instability of Ni/Au based Ohmic contacts have been reported due to Ga out-diffusion and Au inter-diffusion at elevated temperatures [24]. The voltage at which gate leakage current sharply increases (i.e. critical voltage) exhibits a negative temperature dependence with an activation energy of 41.6 meV. The abrupt and permanent gate degradation at elevated temperatures was observed to occur at similar gate leakage currents regardless of critical voltage and stress temperature ($\sim 10^{-7}$ A). Gate leakage currents immediately after critical voltage was reached also displayed similar values at all stress temperatures ($\sim 10^{-6}$ A), indicating similar leakage paths for all stress temperatures.

Pitting and crack formation at the edges of the gate contact have been reported after high reverse gate bias step stress of similar devices [4,6,9,11,12]. However, pitting and cracks do not develop in our devices after gate step stress, though the degradation and electrical signatures are similar to those reported in literature [6,11,12]. Fig. 10 shows the gate leakage current of a typical device during a 60 s step when critical voltage was reached. The sharp increase in gate leakage current does not occur immediately, but displays a time dependence and occurs anywhere from 20 to 40 s after bias is applied. Cross sectional transmission electron microscopy (TEM) of an unstressed device shows an interfacial layer present between the Ni/Au Schottky contact and the GaN cap layer (Fig. 11A). X-ray energy dispersive spectroscopy (EDS), not shown, indicates that this interface is an oxide layer ~15 Å thick, though this layer is too thin for accurate resolution of the oxide species. Oxygen has been shown to be a shallow donor in GaN, with the most favorable defect formation of oxygen substituting for N (O_N). Experimental results have indicated a very low activation energy associated with O_N, ~ 34 meV [25–27]. Additionally, GaN easily forms a native oxide, particularly at elevated temperatures [26]. The unintentional oxide interfacial layer present in our devices is due to processing, from not completely removing the native oxide before depositing Ni for the Schottky contact. Holzworth et al. performed laser assisted atom probe tomography on the Ni/AlGaN interface of an AlGaN/GaN HEMT and also observed an oxide interfacial layer, indicating that the presence of an oxide interfacial layer is not unique to our devices [28].

Time dependent dielectric breakdown (TDDB) is typically observed when the applied electric field, less than the breakdown electric field, is held for a sufficient amount of time. When an electric field is applied to a dielectric, a net electric dipole moment is induced and results in a total dipole moment in the dielectric, or polarization **P**. The polarization can be expressed as

$$\mathbf{P} = \chi \epsilon_0 E_{ox} \tag{1}$$

where χ is the electric susceptibility, ϵ_0 is the permittivity of free space (5.52×10^{-3} e/V Å), and E_{ox} is the electric field on the dielectric.

$$E_{ox} = V_{ox}/t_{ox} \tag{2}$$

where V_{ox} is the voltage drop across the dielectric and t_{ox} is the thickness of the dielectric layer. The local electric field (E_{loc}) experienced by each dielectric molecule is expressed by

$$E_{loc} = E_{ox} + L(\mathbf{P}/\epsilon_0) \tag{3}$$

where L is the Lorentz factor. At breakdown, the resulting current density flowing through the dielectric results in a "localized meltdown," with the breaking of bonds between atoms as the degradation mechanism for TDDB [29–31]. Following the thermochemical electric field model for TDDB in thin SiO_2 films, one can calculate the ionic displacement due to applied electric field [29,30]. Thermal oxidation of GaN has shown the formation of β-Ga_2O_3, a stable polymorph with a monoclinic structure, and can be assumed to be one possible oxide formed at the interface between the Ni-based Schottky contact and the GaN cap layer for our devices [32–35]. One can

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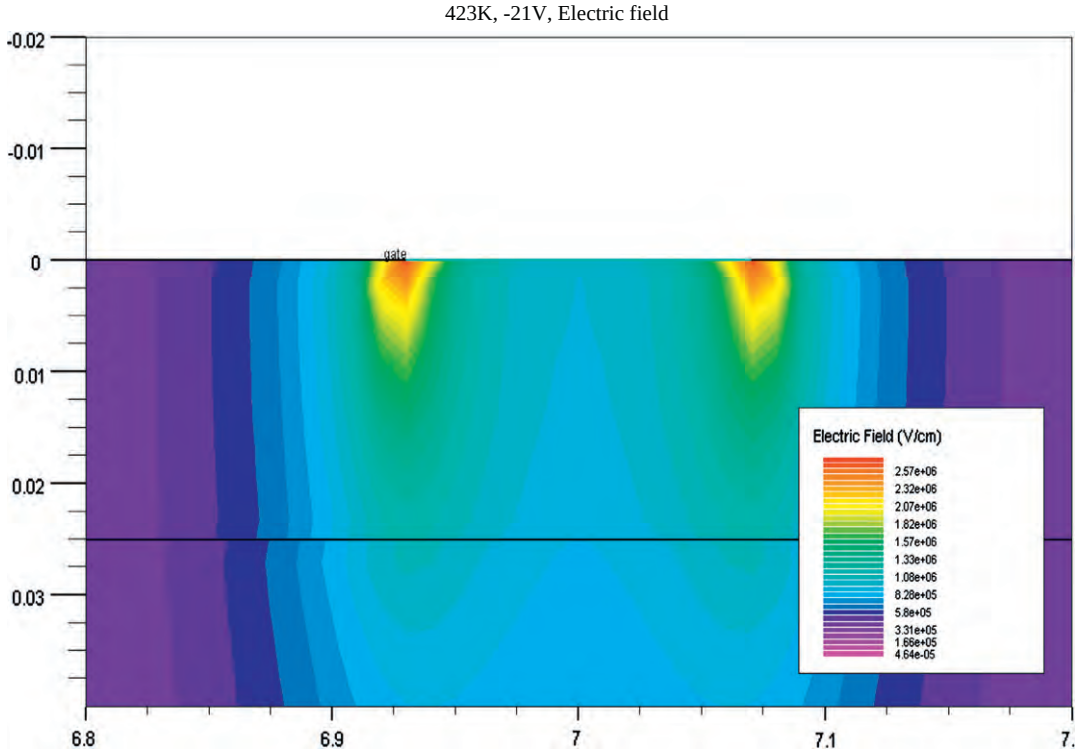

Fig. 6. ALTAS/Blaze 2D simulation of electric field distribution in AlGaN/GaN HEMTs at −21 V at 423 K.

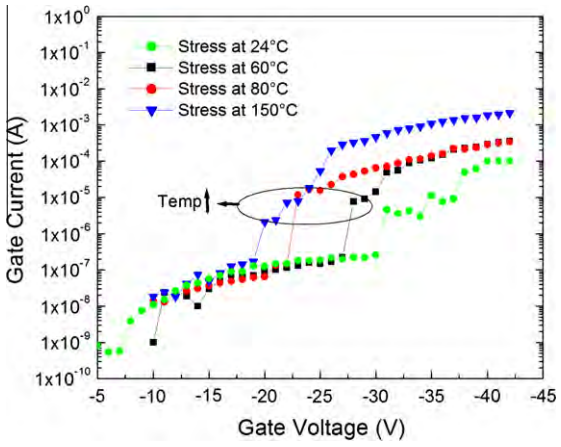

Fig. 7. Gate current of four AlGaN/GaN HEMTs step stressed from −10 V to −42 V at 24 °C, 60 °C, 80 °C, and 150 °C.

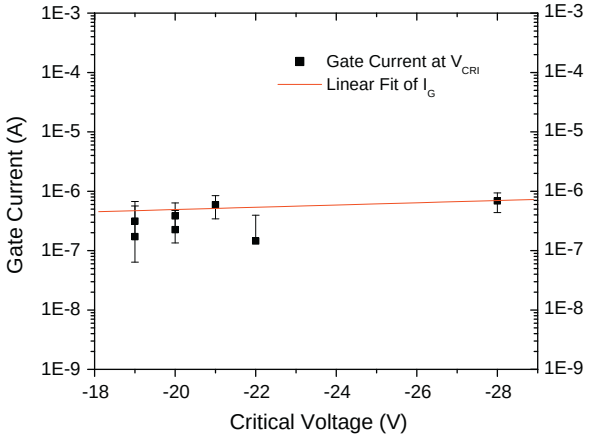

Fig. 8. Gate current dependence on critical voltage of AlGaN/GaN HEMTs measured at V_{CRI}.

calculate the total molecular polarizability from the Clausius-Mossoti relation given by,

$$\alpha = \frac{3(\epsilon_r - 1)\epsilon_0}{(\epsilon_r + 2)N_V} \tag{4}$$

where ϵ_r is the relative dielectric constant for Ga_2O_3 (14.2) and N_V is the number of molecules per unit volume (2.07×10^{22} cm^{-3}) giving a molecular polarizability for Ga_2O_3 of 5.96×10^{-17} e cm^2/V. The total molecular polarizability is comprised of the ionic and electronic component, in which $\alpha = \alpha^i + \alpha^e$. The ionic bond displacement can then, in turn, be calculated by the ionic component of the induced molecular dipole moment Δp^i, where

$$\Delta p^i = \alpha^i E_{loc} \tag{5}$$

Given a very conservative electric field of 2 MV/cm, which is lower than minimum electric field simulated at critical voltage for a stress temperature of 150 °C, this results in a ~10% increase of the Ga–O bond length. A substantial distortion of the ionic bond can result in significant anharmonic coupling to the lattice, increasing the ability for the strained bond to interact with thermal phonons [29,30]. An increase in the stress temperature can provide enough energy to cause the strained ionic bonds to break and lead to breakdown in the dielectric, which contributes to the negative temperature dependence observed for the critical voltage. Once breakdown in the dielectric occurs, a leakage path for electrons can form.

Lo et al. reported on the stability of Ni on GaN investigated by X-ray photoelectron spectroscopy [13]. After an anneal at 300 °C, they observed a decrease in the O–Ga bonding and an increase in

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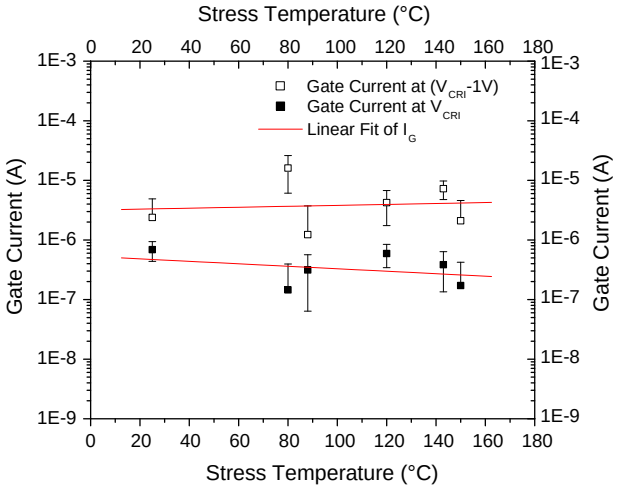

Fig. 9. Gate current dependence on stress temperature of AlGaN/GaN HEMTs measured at V_{CRI} and after V_{CRI} (V_{CRI} – 1 V).

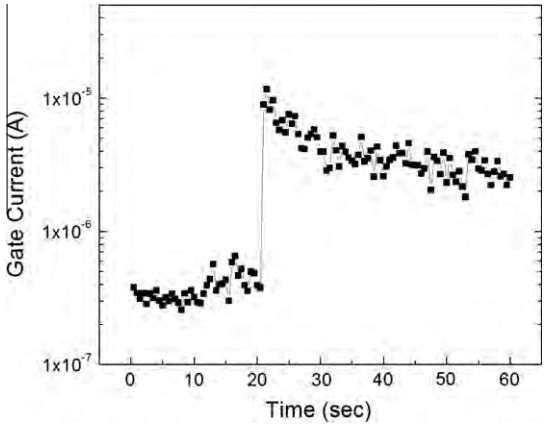

Fig. 10. Gate leakage current during step stress at 24 °C when V_{CRI} occurs (V_{DS} = 0 V, V_{GS} = −30 V).

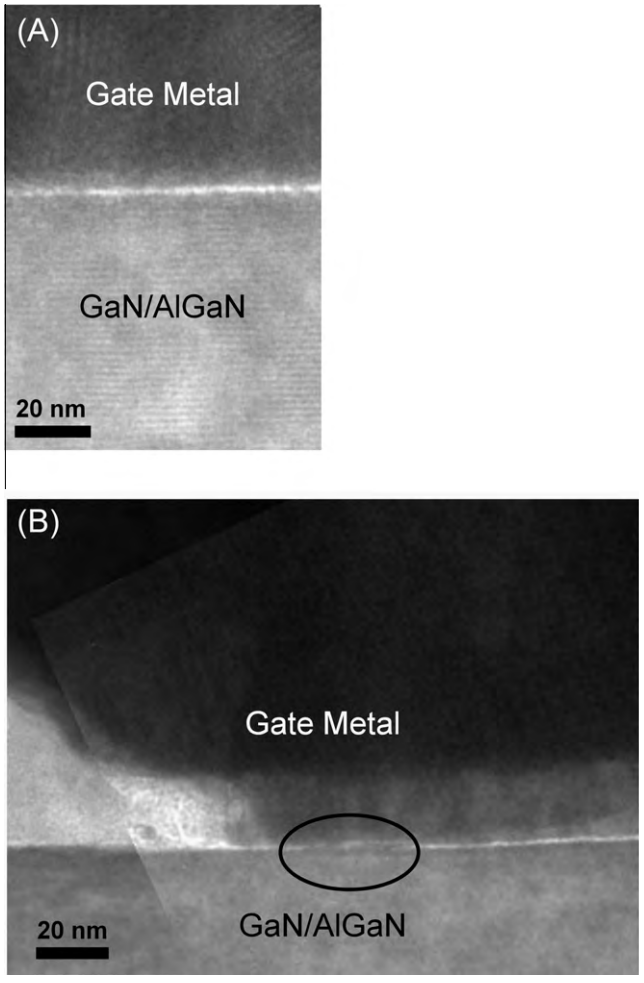

Fig. 11. Cross-sectional transmission electron microscopy image of (A) unstressed device with interfacial layer present, and (B) device step-stressed to y = −42 V at 150 °C. Circled region shows oxide consumption due to stress.

O–Ni bonding through a shift in the Ni 2p and O 1s peak. This indicates that at elevated temperatures Ni will strip oxygen from the native oxide on GaN to create a layer of NiO. It is likely that if oxygen becomes disassociated from Ga during electrical stress because of field induced bond breakage, oxygen will diffuse to form NiO, even at temperatures of 150 °C and lower. Both the intrinsic and piezoelectric induced strain in the GaN cap and AlGaN layer enhance diffusion. Additionally the thermal expansion coefficients of GaN and Ni are considerably different, $5.59 \times 10^{-6}\,K^{-1}$ and $14.17 \times 10^{6}\,K^{-1}$, respectively, resulting in an increase of strain at the interface and further aiding diffusion as the stress temperature increases [36,37]. The breakdown of the interfacial oxide layer due to electric field induced bond breakage, enhanced by thermal and strain effects, results in the consumption of oxide observed from cross sectional TEM after off-state stress, (Fig. 11B), as well as the observed negative temperature dependence on breakdown. A comparison of Ni based and Pt based Schottky contacts during high reverse gate bias step stress on AlGaN/GaN HEMTs was reported by Lo et al. They showed that Pt based Schottky contacts resulted in enhanced stability with no observed breakdown up to −100 V gate step stress, whereas Ni based Schottky contacts showed typical critical voltage breakdown at −55 V [13]. This further reveals that the breakdown occurring at V_{CRI} is dependent upon the reactivity of the gate metal, particularly in the presence of disassociated oxygen.

4. Summary and conclusion

High reverse gate bias step-stress from −10 V to −42 V was performed on AlGaN/GaN HEMTs and resulted in a large increase in gate leakage current, with a sharp one order of magnitude increase in current at the critical voltage. The critical voltage of 0.14 μm gate length devices at room temperature was observed to be −30 V. Over 20 devices were step-stressed at temperatures ranging from 25 °C to 150 °C, exhibiting an activation energy of about 42 meV for the critical voltage. As the stress temperature of the devices increased, the critical voltage was found to decrease linearly. This is due to the breakdown of the interfacial oxide layer from electric field induced bond breakage resulting in the consumption of the oxide interface between the Ni/Au Schottky contact and the GaN cap. Disassociation of oxygen from Ga under high electric fields results in diffusion of oxygen to form NiO_x, likely enhanced by thermal and strain effects. Gate leakage current at V_{CRI} was similar ($\sim 10^{-7}$ A) regardless of stress temperature, indicating similar leakage paths for all stress temperatures. Future work will further investigate the interfacial oxide breakdown by performing both step stress and steady state TDDB voltage testing on AlGaN/GaN HEMTs with unintentional and intentional gate oxides.

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